We claim:

1. A transistor, comprising:
a base;
a collector; and
an emitter comprising a group III/VI semiconductor.

2. The transistor of claim 1, wherein the group III/VI semiconductor is selected from the group consisting of GaS, GaSe, GaTe, InS, InSe, InTe, and TlS.

3. The transistor of claim 1, wherein:
the base comprises a p-type semiconductor material; and
the collector comprises an n-type semiconductor material.

4. The transistor of claim 1, wherein:
the group III/VI semiconductor is doped to behave as a p-type semiconductor;
the base comprises an n-type semiconductor; and
the collector comprises a p-type semiconductor.

5. The transistor of claim 1, wherein the collector comprises a buried collector.

6. The transistor of claim 1, wherein the emitter further comprises an n-type dopant.

7. A microcircuit, comprising:
at least one metal oxide semiconductor (MOS) transistor; and
the transistor of claim 1.

8. A process for manufacturing a BiMOS microcircuit, comprising:

forming a buried layer of a first semiconductor material;

forming a gate oxide for at least one MOS transistor;

forming a poly-Si layer on the gate oxide;

forming a base of a second semiconductor material;

forming a source and a drain for the MOS transistor of a third semiconductor material; and

forming an emitter of a group III/VI semiconductor on the base.

9. The process of claim 8, further comprising:

after forming the buried layer, isolating the buried layer into pockets.

10. The process of claim 8, further comprising forming a deep N+ collector.

11. The process of claim 8, further comprising:

utilizing part of the buried layer as a collector; and

forming contacts to the base, emitter, collector, source, drain, and poly-Si layer on the gate oxide.

12. The process of claim 8, further comprising forming wells of the second semiconductor material in the buried layer.

13. A BiMOS microcircuit produced according to the process of claim 8.

14. A method for relieving mechanical stress between a silicon (Si)-based semiconductor and an electrical contact coupled to the Si semiconductor, comprising:

coupling a group III/VI semiconductor between the Si semiconductor and the electrical contact.

15. The method according to claim 14, wherein the group III/VI semiconductor is selected from the group consisting of GaS, GaSe, GaTe, InS, InSe, InTe, and TlS.

16. A process for manufacturing a heterojunction bipolar transistor (HBT), comprising:

forming a collector of a first semiconductor;

forming a base of a second semiconductor;

forming an emitter of a group III/VI semiconductor;

17. A heterojunction bipolar transistor (HBT) manufactured according to the process of claim 16.

18. The HBT according to claim 17, wherein the group III/VI semiconductor is selected from the group consisting of GaS, GaSe, GaTe, InS, InSe, InTe, and TlS.

19. A transistor, comprising:

a base;

a collector; and

means for providing an emitter with a bandgap greater than 1.1 electron-volts.

20. The transistor of claim 19, wherein the means for providing an emitter further comprises an intrinsic semiconductor.

21. A transistor, comprising:

a base made of a silicon material;

a collector; and

means for providing a non-silicon-based emitter with a flexible structure to relieve lattice mis-match between the emitter and the base.